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1 Session 9: Routing and Clocking: Porosity aware buffered steiner tree construction

Charles J. Alpert, Gopal Gandham, Milos Hrkic, Jiang Hu, Stephen T. Quay

April 2003 **Proceedings of the 2003 international symposium on Physical design**

Full text available: pdf(115.60 KB) Additional Information: full citation, abstract, references, citings, index terms

In order to achieve timing closure on increasingly complex IC designs, buffer insertion needs to be performed on thousands of nets within an integrated physical synthesis system. Modern designs may contain large blocks which severely constrain the buffer locations. Even when there may appear to be space for buffers in the alleys between large blocks, these regions are often densely packed or may needed later to fix critical paths. Therefore, within physical synthesis, a buffer insertion scheme n ...

Keywords: VLSI, buffer insertion, interconnect, physical design

2 Buffered tree construction: A place and route aware buffered Steiner tree construction

C. N. Sze, Jiang Hu, Charles J. Alpert

January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair 2004**

Full text available: pdf(174.37 KB) Additional Information: full citation, abstract, references

In order to achieve timing closure on increasingly complex IC designs, buffer insertion needs to be performed on thousands of nets within an integrated physical synthesis system. In most of previous works, buffers may be inserted at any open space. Even when there may appear to be space for buffers in the alleys between large blocks, these regions are often densely packed or may be useful later to fix critical paths. In addition, a buffer solution may inadvertently force wires to go through rout ...

3 On approximating arbitrary metrices by tree metrics

Yair Bartal

May 1998 **Proceedings of the thirtieth annual ACM symposium on Theory of computing**

Full text available: pdf(4.11 MB) Additional Information: full citation, references, citings, index terms

4 Session 4C: Packing Steiner trees

Kamal Jain, Mohammad Mahdian, Mohammad R. Salavatipour

January 2003 **Proceedings of the fourteenth annual ACM-SIAM symposium on Discrete algorithms**

Full text available: pdf(853.19 KB) Additional Information: full citation, abstract, references, citings, index terms

The Steiner packing problem is to find the maximum number of edge-disjoint subgraphs of

a given graph G that connects a given set of required points *S*. This problem is motivated by practical applications in VLSI layout and broadcasting, as well as theoretical reasons. In this paper, we study this problem and present an algorithm with an asymptotic approximation factor of |*S*|/4. This gives a sufficient condition for the existence of *k* edge-disjoint Steiner trees ...

5 A practical methodology for early buffer and wire resource allocation

Charles J. Alpert, Jiang Hu, Sachin S. Sapatnekar, Paul Villarrubia

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(166.44 KB) Additional Information: full citation, abstract, references, citings, index terms

The dominating contribution of interconnect to system per-formance has made it critical to plan for buffer and wiring resources in the layout. Both buffers and wires must be considered, since wire routes determine buffer requirements and buffer locations constrain wire routes. In contrast to recent buffer block planning approaches, our design methodology distributes buffer sites throughout the layout. A tile graph is used to abstract the buffer planning problem while also addressing wire p ...

6 An enhanced multilevel routing system

Jason Cong, Min Xie, Yan Zhang

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(290.35 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present several novel techniques that make the recently published multilevel routing scheme [19] more effective and complete. Our contributions include: (1) resource reservation for local nets during the coarsening process, (2) congestion-driven, graph-based Steiner tree construction during the initial routing and the refinement process and (3) multi-iteration refinement considering the congestion history. The experiments show that each of these techniques helps to improve the ...

7 Manhattan or non-Manhattan?: a study of alternative VLSI routing architectures

Cheng-Kok Koh, Patrick H. Madden

March 2000 **Proceedings of the 10th Great Lakes symposium on VLSI**

Full text available: pdf(807.78 KB) Additional Information: full citation, abstract, references, citings, index terms

Circuit interconnect has become a substantial obstacle in the design of high performance systems. In this paper we explore a new routing paradigm that strikes at the root of the interconnect problem by reducing wire lengths directly. We present a non-Manhattan Steiner tree heuristic, obtaining wire length reductions of much as 17% *on average*, when compared to rectilinear topologies. Moreover, we present a graph-based interconnect optimization algorithm, called the GRATS-tree algorithm, ...

8 Mathematical programming in a hybrid genetic algorithm for Steiner point problems

David J. Thuente, Pulin Sampat

February 1995 **Proceedings of the 1995 ACM symposium on Applied computing**

Full text available: pdf(763.80 KB) Additional Information: full citation, references, index terms

Keywords: Quasi-Newton method, Steiner points, genetic algorithm, heuristic optimization, mathematical programming

9 The rectilinear Steiner arborescence problem is NP-complete

Weiping Shi, Chen Su

February 2000 **Proceedings of the eleventh annual ACM-SIAM symposium on Discrete algorithms**

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1 **A practical methodology for early buffer and wire resource allocation**
Alpert, C.J.; Jiang Hu; Sapatnekar, S.S.; Villarrubia, P.G.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 22 , Issue: 5 , May 2003
Pages:573 - 583

[Abstract] [PDF Full-Text (668 KB)] **IEEE JNL**